Laboratory Model of the Diode Clamped Four-Level Voltage Source

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Abstract
In the paper, we discuss a laboratory mode of a Diode Clamped 4-level Voltage Source Inverter (VSI) of power approximately 5kVA, that is designed for initial experimental verification of solutions for “software” and “hardware” of the control components in prototype model of inverter 6kV and 0,5-1 MVA. The paper discusses tasks of control console in the PC. The article also discussed construction and development of the power part of the inverter model. In addition, it presents the voltage PWM algorithm implemented in the DSP. Experimental results are presented.

Keywords
Four-level VSI, diode clamped, multilevel inverters, SVPWM, power electronics

Introduction
The recent popular trend in application of the power electronics systems of high power is application of a multilevel inverters [1]. The aim is to achieve voltage with low higher harmonics, as well as to minimize number of power devices such as: transistors IGBT, fast switching diodes or capacitor [2]. Along with development of new typologies, research focuses on development of efficient modulation techniques, which would minimize switches losses or decrease capacitors’ capacities in DC-link circuit [3]. None the less, in the case of high and very high powers, crucial criterion for the choice of inverters is the cost of its elements and its reliability.

The paper discusses laboratory model of the 4-level Diode Clamped VSI, destined for experimental verification of the functional propriety of the solutions and control algorithms implemented in DSP controller. The controller is anticipated to be implemented in prototype of the 4-level inverter of power 0,5-1 MVA and output voltage 6 kV. Sections 2 and 3 present the most important information about experimental stand and power part of the inverter. The following two chapters discuss the algorithm SVPWM realized with DSP controller as well as initial experimental results.

1 Experimental Stand
Block diagram of the experimental stand, that is shown on Fig.1, consists of six fundamental functional blocks. Block {1} consists of a PC with software Visual DSP++ (designing environment for the processor ADSP21363 by Analog Devices) and Quartus (designing environment for the system CYCLONE 2 by Altera), and operator console. From the console level the following inverter parameters are assigned: frequency carrier of the SVPWM, basic frequency of the inverter output voltage, modulation index, dead time, confirmation time of the transistors switching on, amplitude accretion speed of the basic output voltage harmonic. Besides that, the main tasks of the console are: registration and visualization of the selected processor variables, realization of the programming function and formatting of selected memories, diagnostics and event reports as text file. Transmission of the data between the PC and microprocessor controller takes place by separated USB junction with speed 1Mb/s. Blok {2} consists of the microprocessor controller, designed and constructed by „MMB Drives” in Gdansk. The main elements of the controller are: floating point 32-bits processor, working with frequency 333MHz and modern digital programmable FPGA system. The controller is installed in interface board – block {3}, with 20 two-way, optically separated transmission channels, which are used to communicate with IGBT controllers of the VSI (Fig.2).

Fig. 1. Block diagram of the experimental stand

Block {4} presents a group of transistor controllers IGBT. Applied are the controllers IGD515 by CONCEPT company, which are highly integrated control system, with isolated voltage converter and complete light pipe interface. The signal FAULT, from the controller is also the signal that confirms switching on, which is very useful in system’s diagnostics. Digital channels between the controller SH363 and interface board were buffered by HCT systems and LVX. One of the main tasks of the block {5} – connecting apparatus – is preliminary charge of the capacitors in linking inverter circuit. In addition elements protecting from short circuits were installed and connectors allowing quick change of...
the DC-link circuit configuration (for example: input chokes, Z-source, other voltage sources). Measurement block \{6\} consists of a part aggregating measurement signals (current and voltage sensors of type LEM and systems with optical-amplifier HCPL7800) and with analog-digital transducer. Two 14-bits, 4-channels transducers AD7865 by Analog Devices were applied, which allow quick configuration of the measurement channel range from ±5V to ±10V and a choice of number of analog channels to conversion.

2 Power Part of the VSI

The power part of the typical Diode Clamped 4-level VSI is presented on Fig.3. In the experimental model, branches of the inverter were placed at separated radiators. Each of the branches consists of the three transistor modules BSM50GB120DN2 and the three diode modules DD46S12K from the company EUPEC. The three rectifiers are placed on additional radiator. The view of the model’s construction is shown on Fig 4. It is possible to move elements on the radiator and of the radiator which facilitates change of the device typology to for example inverter of type FC (Flying Capacitors). Capacities of the condensers $C_1$-2 equal 1000 µF. The condensers that are not marked on Fig.3, with capacity about 1µF/1200V, function as decoupling capacitors.

3 Modulation Algorithm

To the particular states of the switches of the inverter the appropriate voltage space vector can be selected in stationary coordinates $\alpha$-$\beta$. In the m-level voltage inverters, the area of the space vector is usually divided into 6 sectors, in which we can distinguish triangular areas among three nearest locations of the space vector. Single sector and equilateral triangles of a side $a$ is shown on Fig 5.

Fig. 2. Interface board

Fig. 3. The power part of the typical Diode Clamped 4-level VSI

Fig. 4. Construction of the laboratory model of the Diode Clamped 4-level VSI

Fig. 5. Single sector for m-level VSI

Reference voltage vector $V$ can be presented as linear combination of the vectors $i$ and $j$. In accordance with Fig. 4 coordinates $[\alpha, \beta]$ of vector $V$ are as follows:
\[ \vec{V} = [\alpha, \beta] = m \cdot \vec{i} + n \cdot \vec{j} \]  \hspace{1cm} (1)

where:

\[ m = \alpha / a - \beta / (a\sqrt{3}) \quad \text{and} \quad n = 2 \cdot \beta / (a\sqrt{3}) \]  \hspace{1cm} (2)

Integer of the \(m\) and \(n\) define coordinates of beginning of parallelogram \(P\) (point \(PR\) on Fig.5), where reference vector occurs at the time. In order to determine belonging of the reference vector \(V\) to one of the two triangles in parallelogram \(P\), the value of the following sum \(D\) needs to be found out:

\[ D = [m - \text{int}(m)] + [n - \text{int}(n)] \]  \hspace{1cm} (3)

If \(D \leq 1\), then the reference voltage vector \(V\) occurs in the triangle with index \([m][n]_1\), else the vector \(V\) belongs to the triangle with index \([m][n]_2\). Finally, the synthesis of the reference vector \(V\) consists on addition of several states of switches, during modulator’s work, according to order defined in control strategy.

There exist two possible positions of the vector \(V\) in the parallelogram \(P\) (Fig.6). Reference vector \(V\) can be projected within area of each of the two triangles.

\[ \vec{V} = \frac{p_1(\vec{V}_1 - \vec{V}_3)}{\vec{p}_1} + \frac{p_2(\vec{V}_2 - \vec{V}_3)}{\vec{p}_2} + \vec{V}_3 \]  \hspace{1cm} (4a)

\[ = p_1\vec{V}_1 + p_2\vec{V}_2 + (1 - p_1 - p_2)\vec{V}_3 \]  \hspace{1cm} (4b)

where: \(p_1, p_2\) – relative lengths (time duration) of the active vectors \(V_1\) and \(V_2\).

Time duration of zero vectors \(V_1\) and \(V_2\) result from a difference in modulation time and duration of the active vectors. All space vectors of the 4-level VSI are presented on Fig.7.

![Fig. 7. Space vectors of the 4-level VSI](image)

In the selected sector 0 on the Fig.7 occurs nine, numbered regions. Specified position of the space vector is coded as follows– given number defines a point in the linking circuit connected to a load terminal of the particular phase (from left \(a, b, c\)). For example, the code „321” means, that the phase \(a\) was linked to voltage source of value \(3(U_{DC}/3)\), phase \(b\) was linked to the voltage source of value \(2(U_{DC}/3)\), and phase \(c\) was linked to the voltage source of value \(1(U_{DC}/3)\). In case of linear modulation range, value of maximum phase voltage equals \(\sqrt{3}(U_{DC}/3)\), and maximum value of normalized modulation factor in this case equals \(3\sqrt{3}/2\).

![Fig. 8. Example of the position of the normalized vector V in the region 4](image)

Fig.8 provides exemplary positions of the space vector of four-level inverter. When the reference
vector $V$ occurs in the region 4, relative lengths of the space vectors $V_{133}=V_{220}$ and $V_{321}=V_{210}$ equal:

$$p_1=2-n;\ p_2=1-m$$

(5)

Hence, the vector-duty factors for particular positions of the space vector in modulation period are as shown in the Table 1.

**Table 1. Vector-duty factors for regions 1-9 on Fig.8**

<table>
<thead>
<tr>
<th>Reg.</th>
<th>Duty factors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$d_{200/311}=3\cdot m-n$ ; $d_{310}=m-n$</td>
</tr>
<tr>
<td>2</td>
<td>$d_{200/311}=1\cdot n$ ; $d_{210/321}=2\cdot m$ ; $d_{310}=m+n\cdot 2$</td>
</tr>
<tr>
<td>3</td>
<td>$d_{210/321}=3\cdot m-n$ ; $d_{310}=m-1$ ; $d_{320}=n-1$</td>
</tr>
<tr>
<td>4</td>
<td>$d_{210/321}=2\cdot n$ ; $d_{220/331}=1\cdot m$ ; $d_{320}=m+n-2$</td>
</tr>
<tr>
<td>5</td>
<td>$d_{220/331}=3\cdot m-n$ ; $d_{330}=n-2$ ; $d_{320}=m$</td>
</tr>
<tr>
<td>6</td>
<td>$d_{100/211/322}=2\cdot m-n$ ; $d_{200/311}=m-1$ ; $d_{200/321}=n$</td>
</tr>
<tr>
<td>7</td>
<td>$d_{110/221/332}=1\cdot m$ ; $d_{210/321}=m+n-1$</td>
</tr>
<tr>
<td>8</td>
<td>$d_{110/221/332}=2\cdot m-n$ ; $d_{210/321}=m$ ; $d_{220/331}=n-1$</td>
</tr>
<tr>
<td>9</td>
<td>$d_{100/111/222/333}=1\cdot m-n$ ; $d_{100/211/322}=m$ ; $d_{110/221/332}=n$</td>
</tr>
</tbody>
</table>

**Fig. 11. Load current $i_w$, $i_b$, $i_c$ and phase voltage $u_a$ (output $f_v=50$ Hz, carrier $f_c=4$ kHz, relative modulation factor $m_a=1.55$)**

**Fig. 12. Load current $i_w$, $i_b$, $i_c$ and phase voltage $u_a$ (output $f_v=60$ Hz, carrier $f_c=800$ Hz, relative modulation factor $m_a=1.55$)**

**5 Summary**

Presented oscillograme on the Fig.9÷Fig.12 regards preliminary phase of the experiment, where unloaded squirrel-cage motor was used. The purpose of this research was verification of the solution for the constructed laboratory model of the 4-level VSI, verification of the application of the DSP controller with own interface card, and investigation of the propriety of implemented algorithms. Therefore, so far, supply of the linking circuit has been solved differently than it is shown on the Fig.3 (rectifier bridges).

Preliminary experimental results confirm propriety of suggested modulation strategy and applied solutions. The research and improvement of the model and the algorithm will be continued in order to implement analog solutions in constructed prototype of the 4-level voltage inverter 6kV/0,5-1 MVA, based on converters IGBT FD200R65F1-k and FZ200R65kF1.

**References**