Simulation investigation of the Z-source NPC inverter

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Abstract
The paper describes construction and the principles of activity, attributes and potential of 3-phase Z-type inverters. The paper focuses on the basic system and suggested 3-level system of a NPC type Z-inverter, which was elaborated by authors. Simplified theoretical analysis of both systems has been verified by detailed simulation research. In the last section of the article, the possibility to build multilevel Z-inverters based on Diode Clamped typology is presented.

Keywords
Power electronics, boost-buck converter, Z-inverter, NPC-inverter

Introduction
Alternating Voltage Inverters (Converters) supplied by low-voltage sources DC (ex. fuel cell, photovoltaic cell) are most frequently realized on the basis of the three fundamental typologies: a) PWM voltage inverter with non-transformer converter DC/DC in the „boost-converter” system, b) PWM voltage inverter with transformed converter DC/DC in the „boost-converter” system, c) PWM current converter. However none of these solutions is allowed (permitted) states: six „active” states (while exchange of instantaneous power between the load and DC circuit) and two „null” states (when the load is shorted by lower or upper group of transistors). Whereas, 3-phase Z-inverter system (fig.1) can assume nine permitted states, that is one more than in VSI system. Additional ‘ninth’ state is the third “null” state, occurring when the load is being shorted simultaneously by lower and upper group of transistors. This state, is defined as „shoot-through” state and may be generated in seven different ways, however equivalent procedures: independently through every branch (3 procedures), simultaneously through two of the branches (3 procedures), simultaneously through all of the three branches (1 procedure). The main, unique characteristic of Z-inverter is that shoot-through state permits to rise output voltage, above the supply voltage U_{DC}.

Source Z serves as power storage and guarantees double filtration grade at the input of the inverter, and therefore dumping current ripples and voltage pulsation in the DC circuit. Concluding, requirements for chokes and capacitors in Z-source are less restrictive than in VSI or CSI inverters. In a case where chokes L_{1} and L_{2} have very low inductance (≈0), Z-source is created only from parallel connected capacitors C_{1} and C_{2}. Then Z-inverter simply becomes VSI system and condensers in DC circuit are the only storage for energy and at the same point are a cell for filtration of voltage pulsation. Analogically when capacitors C_{1} and C_{2} are of low capacity (≈0), Z-source is diminished to two chokes L_{1} and L_{2} that are parallel connected, and Z-inverter system becomes CSI system. Chokes in DC circuit of CSI system and capacitors in DC circuit of VSI system must be of greater inductance and capacity (their dimensions) than in case of Z-inverter.

Fig. 1. Basic scheme of the 3-phase Z-inverter

Typical 3-phase VSI system can assume eight allowed (permitted) states: six „active” states (while exchange of instantaneous power between the load and DC circuit) and two „null” states (when the load is shorted by lower or upper group of transistors). Therefore application of Z-inverter is possible only where there is no necessity for energy return to U_{pump} source, further it is even forbidden in case of fuel cell or photo-voltaic cell. It should be marked that same as D diode function can be server by other power electronics systems including ex. diode rectifier or typical „boost-converter”.

1 Work principles of Z-type inverter

Figure 1. presents a scheme of basic 3-phase Z-inverter. In distinction from VSI and CSI inverters, on DC side of Z-inverter occurs a D diode and a Z-source of “X” shape, composed of two capacitors C_{1} and C_{2} and two chokes L_{1} and L_{2}. The D diode prevents forbidden reversed current flow. For this reason application of Z-inverter is possible only where there is no necessity for energy return to U_{pump} source, further it is even forbidden in case of fuel cell or photo-voltaic cell. It should be marked that the same as D diode function can be server by other power electronics systems including ex. diode rectifier or typical „boost-converter”.
Figure 2. describes simple equivalent schemes of Z-inverter, examined from the clap site of DC, where a source $u_s$ shapes inverter bridge $V_1-V_6$ (Fig.1). In the shoot-through states (Fig.2b) a D diode is polarized reversely and does not conduct the inverter bridge input voltage $u_d=0$, and energy stored in capacitors $C_1$ and $C_2$ is transferred to the chokes $L_1$ and $L_2$. In „non-shoot-through” states, where every combination of the chokes $V_1-V_6$ that is allowed in VSI system is possible, the D diode conducts, and the voltage $u_d$ increases stepwise from 0 to its maximum $u_k^*$. Since Z-source is symmetric circuits (Fig.2), when $C_1=C_2$ and $L_1=L_2$ and low voltage pulsation $u_{c1}$ and $u_{c2}$ during impulse period $T$, it can be recorded:

$$u_{c1} = u_{c2} = U_C, \quad u_{L1} = u_{L2} = u_L$$  \hspace{1cm} (1)

a) general 

b) in shoot-through” states 

c) in states „non-shoot-through” states

Fig. 2. Equivalent schemes of the Z-inverter

If taken into consideration, that in a time period $T=T_s+T_N$, in steady state overage voltage in chokes $U_L=0$, then on the basis of (2) and (3) we obtain:

$$U_L = \frac{T_z \cdot U_C + T_N \cdot (U_{IN} - U_C)}{T} = 0$$  \hspace{1cm} (4)

and

$$U_C = U_d = U_{IN} \cdot \frac{T_N}{T_N - T_z} = U_{IN} \frac{1 - D}{1 - 2 \cdot D}$$  \hspace{1cm} (5)

where: $D=T_z/T$ - „shoot-through” coefficient, satisfying a condition $D<0.5$.

Similar procedure, on the basis (3) and (4) determines the value $u_{k}^*$ of voltage $u_d$ in „non-shoot-through” states:

$$u_{k}^* = U_C - u_L = U_{IN} \cdot \frac{1}{1 - 2 \cdot D}$$  \hspace{1cm} (6)

where: $1/(1-2 \cdot D) = T/(T_s+T_z) \geq 1$ – peak factor, determining the value $u_{k}^*$ voltage $U_{IN}$.

The value $u_{k}^*$ determines output voltage amplitude $u_{OUT(max)}$ of Z-inverter. When applying sinusoidal PWM algorithm the amplitude equals:

$$u_{OUT(max)} = M \cdot \frac{u_{k}^*}{2} = M \cdot \frac{U_{IN}}{1 - 2D}$$  \hspace{1cm} (6)

where: $M$ – modulation index, of maximum value limited by inequity $M \leq 1-D$, related to time $T_z$ of „shoot-through” states

As it results from the equation (6), Z-inverter output voltage amplitude $u_{OUT(max)}$ can be as well lower as higher than in typical VSI system with sinusoidal PWM, e.g. $u_{OUT(max)}=M \cdot U_{IN}/2$. This possibility is acknowledged when looking at the 3D diagram of dependences:

$$K = \frac{u_{OUT(max)}}{U_{IN}/2} = \frac{M}{1 - 2D}$$  \hspace{1cm} (7)

in domain $\Omega= (0 \leq M \leq 1; \; D < 0.5 \cap D \leq 1-M)$ acceptable changes of $D$ and $M$, presented at the Figure 3.

2 Results of simulation of the Z-inverter

Simulation research of the system (Fig.1) was conducted in software package: PSIM Professional. To
control chokes $V_1$-$V_n$ algorithm of sinusoidal PWM was applied, modified by „shoot-through” states. The essence of this modification is explained on the Fig. 4. Selected results of the research are presented on the Figures 5-8. Elementary parameters of the system that were assumed in the research are presented in Table 1. Any changes of these parameters are described by equivalent diagrams.

Table 1. Parameters of researched Z-inverter (Fig.1)

<table>
<thead>
<tr>
<th>Supply DC</th>
<th>$U_{IN}$</th>
<th>150V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z-source</td>
<td>Chokes</td>
<td>$L_1$, $L_2$</td>
</tr>
<tr>
<td></td>
<td>Capacitors</td>
<td>$C_1$, $C_2$</td>
</tr>
<tr>
<td>Output</td>
<td>Chokes</td>
<td>$L_f$</td>
</tr>
<tr>
<td>filter</td>
<td>Capacitors</td>
<td>$C_f$</td>
</tr>
<tr>
<td>Load (resistance)</td>
<td>$R_0$</td>
<td>6 Ω</td>
</tr>
<tr>
<td>PWM frequency carrier</td>
<td>$1/T$</td>
<td>10 kHz</td>
</tr>
</tbody>
</table>

Conduct simulation research of Z-inverter confirmed theoretical dependence (7) with great accuracy. Small error did not depended on assumed values of loads $R_0$ and parameters $L_1=L_2$ and $C_1=C_2$ of Z-source, and a harmonic distortion coefficient in input voltage $u_{OUT}$, that was counted each time, have never crossed 3%. The research also showed that transitions in Z-inverter, resulting from changes of load $M_{LOAD}$ and factors $M$ and $D$ (in open control system) are relatively fast. Furthermore, they inspired the author to elaborate and conduct preliminary simulation research of 3-level Z-NPC inverter. A premise to do the research was that it is impeded to increase of output voltage amplitude of Z-inverter over 10-times value of supply voltage $U_{IN}$.

Fig. 4. Simple Control algorithms implementing in simulation models of the Z-inverter

Fig. 5. Selected voltages and currents in case of changes of resistance load $R_0$ ($M\equiv D=0.48$)

Fig. 6. Selected currents and voltages before and after change of coefficient $D=0.48 \rightarrow 0.47$ for the time $t=10$ ms ($M=0.48$)

Fig. 7. Voltages and currents at the characteristic points of the system (Fig.1) in the time $\Delta t_m$ marked at the Fig.6
3 Z-NPC Inverter

Proposed system of 3-level Z-NPC inverter [2] is presented on the Figure 9. Instead of two voltage sources or two capacitors with common point, as it applies to typical systems VSI-NPC [3], in this inverter two Z-sources with input voltage $U_{IN1}$ and $U_{IN2}$ without common point were applies. This allows joint and separated voltage $u_d$ control. The possibility is explained by equivalent diagrams of Z-NPC inverter in „short-trough” states, showed at the Figure 10.

![Diagram of Z-NPC Inverter](image)

**Fig. 9. Proposed system of 3-level Z-NPC inverter**

In the state of „short-trough” upper branches (Fig.10-b1), transistors $V_1$-$V_6$ & $V_1'$-$V_6'$ are attached, however in states of „short-trough” lower branches (Fig.10-b2) transistors $V_1''$-$V_6''$ & $V_1''$-$V_6''$ (Fig.9). These two states with the duration time $T_Z$ and $T'_Z$ in time period $T$ (Fig.11), cause averages voltages increase $U_c$ and $U_d$, and maximal $u_d$ up to value:

a) on output of upper $Z_1$-source

$$U_c = U_{d1} = U_{IN1} \cdot \frac{1 - D}{1 - 2 \cdot D}$$  \hspace{1cm} (8)

$$u_{d1} = U_{IN1} \cdot \frac{1}{1 - 2 \cdot D}$$

b) on output of lower $Z_2$-source

$$U_c' = U_{d2} = U_{IN2} \cdot \frac{1 - D'}{1 - 2 \cdot D'}$$

$$u_{d2} = U_{IN2} \cdot \frac{1}{1 - 2 \cdot D'}$$  \hspace{1cm} (9)

where: $D = T_d/T$ and $D' = T'_d/T$ - „short-trough” coefficients of upper and lower branches.

![Diagram of Z-NPC Inverter](image)

**Fig. 10. Equivalent schemes of the Z-NPC inverter: a) general, b) in states of „short-trough”: upper branches (b1), lower branches (b2) and full (b3)**

Occurring physical process and following deduced dependences (8) and (9), are analogical to those in a basic system of Z-converter (Fig.1) and the equations (4) and (5). It is also unchanged by full „short-trough” state (Fig.10-b3), occurring when short circuit of upper and bottom branched happen simultaneously at the time $T_Z - AT_Z$ (Fig.11).

![Diagram of Z-NPC Inverter](image)

**Fig. 11. Exemplary schedule of branches “short-trough” in T period**

Considering Z-NPC inverter, which is supplied by a source of different voltage $U_{IN1} \neq U_{IN2}$ and controlled on the basis of sinusoidal PWM, and taking into account (8) and (9), we can determine input voltage peak-to-peak value on the basis of the following dependence:
\[ u_{OUT}(p) = \frac{M}{1-2D} \cdot \frac{U_{IN1}}{1-2D} + \frac{M'}{1-2D'} \cdot \frac{U_{IN2}}{1-2D'} \] \tag{10}

where: \( M \) and \( M' \) – modulation index for positive and negative half of output voltage.

Hence, if the following condition is not fulfilled:

\[ M \cdot \frac{U_{IN1}}{1-2D} = M' \cdot \frac{U_{IN2}}{1-2D'} \] \tag{11}

then the voltage \( u_{com} \) between reference potential \( V_0 \) (Fig.9) and a common point of symmetric 3-phase load (e.g. DC-offset):

\[ u_{com} = V_0 - \frac{2}{\pi} \left( M \frac{u_{d1}^*}{2} - M' \frac{u_{d2}^*}{2} \right) \] \tag{12}

is different than ‘zero’. Then, in output voltage occur additional distortion, mainly related to even harmonics.

Meeting condition (11), that eliminates input voltage distortion and DC-offset, is possible through: a) selection of different modulation index’s \( M \) and \( M' \) for the positive and negative half; b) selection of different ‘short-trough’ coefficient \( D \) and \( D' \) for upper and bottom branches. In the first case, where \( D=D' \) and the following ratio remains valid:

\[ \frac{M}{M'} = \frac{U_{IN2}}{U_{IN1}} \] \tag{13}

voltage amplitude \( u_{OUT} \) can be varied within the limits:

\[ 0 \leq u_{OUT(max)} \leq \frac{1}{2(1-2D)} \cdot \min(U_{IN1}, U_{IN2}) \]

Whereas, in the second case, where \( M=M' \) and the following ratio remains valid:

\[ \frac{(1-2D')}{(1-2D)} = \frac{U_{IN2}}{U_{IN1}} \] \tag{14}

the amplitude can vary within the limits:

\[ 0 \leq u_{OUT(max)} \leq \frac{U_{IN1}}{2(1-2D)} = \frac{U_{IN2}}{2(1-2D')} \]

where maximal voltage in transistors \( V_{1,2} \) \( V_{3,4} \) \( V_{5,6} \) \( V_{7,8} \) (Fig.9) are equal. Evidently it is the possibility to joint both procedures to meet condition (11).

### 4 Research results of the Z-NPC inverter

Parameters for the simulated Z-NPC system were assumed analogically to the Z-type inverter (Tab.1). Eventual changes of the parameter are marked at the Figures 13-17, presenting the most important simulation research results, conducted in the software package PSIM Professional. The research confirmed correct work of Z-NPC inverter (Fig.9) with the system’s power supply from sources for equal as well as different voltage \( U_{IN1} \) and \( U_{IN2} \) (Fig.12-Fig.15).

In each case, when \( U_{IN1}=U_{IN2} \), content of harmonics in voltage \( u_{OUT} \) is like in basic Z-inverter system (Fig.1). Similarly run also transitory processes (Fig.12, Fig.15). Perceptible are only somewhat greater low-frequency voltage and current pulsations in Z-sources of Z-NPC inverter (compare Figure 5, and Figure 12). This is also characteristic, however to less extent, of typical NPC-VSI system with capacitor supply voltage divider. When supplying Z-NPC system from sources with voltage \( U_{IN1} \neq U_{IN2} \), selection of „short-trough” coefficients upper branches \( D \) and bottom branches \( D' \) satisfy relation (14) appeared to be a effective method to eliminate output voltage distortion \( u_{OUT} \) and DC-offset (Fig.13-Fig.15). Such a coefficients’ selection, as expected, caused also maximal voltages compensation in the transistors \( V_{1,2} \) \( V_{3,4} \) \( V_{5,6} \) \( V_{7,8} \) and output voltage impulse amplitude \( u_{F(a)} \) directly at the inverter terminals (Fig.13, Fig.16).

![Fig. 12. Selected voltages and currents in Z-NPC inverter after enclosure and after change of „short-trough” coefficient D=0,48→0,47 at the moment t=10 ms (M=0,48)](image)

### 5 Conclusions

As one concludes from the article, Z-source could be successfully applied in multilevel inverters realized on the basis of typology „Diode Clamped”. As example serves the system presented at the Figure 17. It is necessary to notice that when inverters with Z-sources are supplied by diode rectifiers from alternating voltage grid, then there is no need to use neither capacity filters nor input diodes of inverters.

Presented results encourage to continue research on systems with Z-sources, especially in practical
aspect. The authors would like to draw attention to the requirements for accuracy of realized controllers, related to sensibility of described systems to changes of “short-trough coefficients.

a) equal coefficients \( D_1 = D_2 \)

b) after \( D_2 \) coefficients correction on the basis (14)

Fig. 13. The output phase voltage, DC-offset voltage and output voltage \( U_{in} \) in the inverter terminals, in case of differentiated voltages \( U_{IN1} \# U_{IN2} \)

Fig. 14. The output phase voltages and DC-offset in case: a) equal \( U_{IN1} = U_{IN2} \) and \( D_1 = D_2 \); b) differentiated \( U_{IN1} \# U_{IN2} \) and equal \( D_1 = D_2 \); c) differentiated \( U_{IN1} \# U_{IN2} \) and after correction of coefficient \( D_2 \) on the basis of dependence (14)

Fig. 15. The courses of output phase voltages and DC-offset voltage, in case of stepwise changes of work conditions for Z-NPC inverter selected on the figures 14 a,b,c

Fig. 16. The voltage impulses on input and output terminals of a Z-NPC inverter in the case presented at figure 15c

Fig. 16. 4-level Z-inverter system of DC type

References


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